Amendments to the Claims:

This listing of claims is submitted to replace the prior version claims in the application:

Listing of Claims

1-4. (Canceled).

5. (Currently Amended) A ferroelectric memory comprising:

a sense amplifier; and

a memory unit, coupled to the sense amplifier, comprising:

a positive bit line and a negative bit line which are parallel to each other and are coupled to the sense amplifier;

a word line which is virtually perpendicular to the positive and the negative bit lines;

a positive memory cell which is coupled to the word line and will be connected to the positive bit line when the word line is enabled;

a negative memory cell which is coupled to the word line and will be connected to the negative bit line when the word line is enabled;

a plate line which is coupled to the positive and the negative memory units;

a first current source which is coupled to the positive bit line; and

a second current source which is coupled to the negative bit line, wherein, while reading the memory cell, the first current source supplies a first current to the positive bit line and the second current source supplies a second current to the negative bit line before the sense amplifier is activated for enlarging the voltage difference between the positive bit line and the negative bit line.

6. (Original)The ferroelectric memory according to claim 5, wherein the ferroelectric memory is applied in a plate-line driven access method, of which, the first current source flows to ground from the positive bit line while the second current source flows to ground from the negative bit line.

7. (Original) The ferroelectric memory according to claim 6, wherein the first current source and the second current source, which individually comprise an N-type transistor, are conducted according to an over-driven signal.

8. (Original) The ferroelectric memory according to claim 5, wherein the ferroelectric memory is applied in a bit-line driven access method, of which, the first current source flows to the positive bit line while the second current source flows to the negative bit line.

9. (Original) The ferroelectric memory according to claim 8, wherein the first current source and the second current source, which individually comprise a P-type transistor, are conducted by an over-driven signal.

10. (Original) The ferroelectric memory according to claim 5, wherein the sense amplifier is a latch sense amplifier.

11-15. (Canceled).